PARESH RAMDAS DUKARE

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EDUCATION

College of Engineering Pune, Maharashtra	*August 2019 - Present*
MTech in VLSI and Embedded System	CGPA : 7.46
Government College of Engineering,Jalgaon, Maharashtra	*June 2018*
BTech in Electronics and Telecommunication	CGPA:8.40
Gandhigram College,Wardha,Maharashtra	*May 2014*
Class XII (INTEREMEDIATE)	Percentage : 74.77
Agragami High School Wardha, Maharashtra	*May 2012*
Class X (MATRICULATION)	Percentage : 97.45

TECHNICAL SKILLS

Languages	C , C++ , Python(beginner)
Hardware Descriptive Languages	Verilog , SystemVerilog, UVM(beginner)
Tools/Softwares	EDA Playground, Xilinx ISE, Questasim, NgSpice

PROJECTS

Development of AMBA ACE Protcol UVC
Tech Stack Questasim
In this project,I'm designing and developing ACE signals by extending AXI4 and AXI5 Protcol using system verilog UVM based Verification.There will be BFM to connect ACE interface with other slave components such as programmable cache memory.

Accident Detection and Messaging System using GSM and GPS Modules
Tech Stack   Arduino board,Microcontroller Atmeg 328p.
In this project, we have embedded microcontroller in arduino board.When accident occuurs, vibration sensor gets disturbed and gps tracks the location of site and through gsm sends emergency message to nearby ambulance service through microcontroller.

INDUSTRIAL EXPERIENCE

Semi Custom design flow Using MentorGraphics EDA tools	*17 April 2020*
CoreEL Technologies in association with Mentor Graphics, Bangalore	
System Verilog and UVM based Verification using QuestaSim tool	*29 June 2020*
CoreEL Technologies in association with Mentor Graphics, Bangalore	

RELEVANT COURSES

Digital Electronics, RTL,VLSI Design verfication and Testing,Digital CMOS, Analog Electronics,Embedded System, Communication.

ACADEMIC AWARDS AND ACHIEVEMENTS

NPTEL Online Certification:Introduction to Internet of Things

Receiving Monthly scholarship from AICTE for clearing GATE 2019 exam(score:449)

Runner up in Circuit Frenzy at Technoarena national level technical event

Runner up in Quiz Competition at Technoarena national level technical event

POSITION OF RESPONSIBILITIES

Working as a Teaching Assistant for laboratory courses of 1st year M.Tech and 3rd year B.Tech Electronics and Telecommunication.

Worked as a team member in organizing events such as Paper Presentation, Circuit Frenzy, Spurious Quest

Hospitality Committe Coordinator at Abhivyakti Cultural Fest.

EXTRA-CURRICULAR ACTIVITIES

Cricket,Movies

General Knowledge Debates

Exploring new places and Trekking