

# Meghana Padagatti

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## SUMMARY

To enhance my educational and professional skills in a stable and dynamic workplace

## SKILLS

Microsoft office	<div style="width: 75%;"></div>	Manual testing	<div style="width: 75%;"></div>
Power BI	<div style="width: 75%;"></div>	Tableau	<div style="width: 75%;"></div>
SQL	<div style="width: 75%;"></div>	Operating systems	<div style="width: 75%;"></div>

## EDUCATION

**Mtech (72%)**  
KLE's BVBCET Hubli *2016 - 2018*

**BE (ECE 63%)**  
TCE Gadaga *2012 - 2016*

**PUC (74.16%)**  
KLE PU Science college Hangal *2010 - 2012*

**SSLC(89%)**  
JGHS Hangal *2010*

## PROJECTS

### RTL to GDS flow, Design of 32 bit counter (VLSI Physical design flow)

We will start by coding a design in VHDL or Verilog. We will simulate the coded design, followed by design synthesis and optimization then run equivalency checks at different stages of the flow. After synthesizing the design, we will floorplan, and place-and-route the synthesized netlist while meeting timing. We will run gate-level simulation throughout the flow. Finally, you will write out a GDSII file.

### Implementation of 6T, 8T and 10T full adder at 180nm Technology.

Proposed adders gives higher performance than most of the adder as it consumes less silicon area lowest transistor count and also it operates at a low voltage and yet giving a good speed. Project was done in Cadence Virtuoso tool and Micro wind.

### RFID Based classroom attendance system

To verify the identity or attendance of the user Using RFID card and RFID card reader. It was implemented using MATLAB tool .

### Compatibility testing and Usability testing project

In Compatibility testing,we test the functionality of an application in different software and hardware environment while in usability testing we test whether application is user friendly or not.

## LANGUAGES

English



Kannada



Hindi



## AWARDS AND FELLOWSHIP

**Master's Fellowship (2016-2018).**

**Bachelor's Fellowship (2012-2016)**