

# ARATHY M S

## DESIGN VERIFICATION ENGINEER



### CONTACT

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Meenangadi, Wayanad

Kerala, India

### TECHNICAL KNOWLEDGE

- C Programming
- Verilog
- System Verilog
- RTL Designing
- UVM

### SOFTWARE SKILLS

- Questasim
- Vivado
- MS office

### STRENGTHS

- Dedication
- Quick learner
- Self Confident
- Friendly and interactive

### PERSONAL PROFILE

Date of Birth 17/01/1998

Age 23

Nationality Indian

Marital Status Unmarried

Blood Group B+ ve

Known languages Malayalam, English, Tamil

Hobbies Mentoring, Listening music, Dancing, Yoga

### TRAINING AND INTERNSHIPS

- 2020 completed professional course in vlsi designing and verification
- 2018 IOT Application-node in Pantech solutions, Ernakulam
- 2017 BEC Training Program
- 2017 Internship on Telecom technologies at BSNL, Kannur
- 2016 IETE sponsored workshop on Arduino
- 2015 Internship at Telecom of BSNL, Thiruvananthapuram

### ACADEMICS

- B Tech** APJ AbdulKalam Technological University, 2019  
Vimaljyothi Kannur dist  
Kerala, India  
CGPA: **6.86**
- Diploma** Kerala Technical Board, 2016  
Govt. Polytechnic, Meenangadi  
Wayanad dist, Kerala, India  
CGPA: **8.17**
- Class 12<sup>th</sup>** NIOS, 2015  
India  
Percentage: **60%**
- Class 10<sup>th</sup>** Technical Board, 2013  
Govt. Technical school, Sulthan Bathery  
Wayanad dist, Kerala, India  
Percentage: **97%**

### EXTRA-CURRICULAR ACTIVITIES

- Candidated as vice chairman
- IETE Volunteer 2015-2017.
- NSS Volunteer
- Arts committee executive member

### PROJECTS

- Dual elevator using verilog
- NRF based speed limiter with automatic dimming light
- Automatic parking system using c
- Designed HDLC Deframer
- Boot's multiplier
- Remote controlling on home appliances