Vishal **Muley**

L-56, LIG Qtrs Infront of basket ball ground near Ambedkar garden, Nagpur, Maharashtra, 440017, INDIA

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"Hard work beats talent when talent doesn't work hard."

Objective

Seeking a challenging position in the field of VLSI Design and Communication where I can contribute my skills and knowledge for the organization's success and synchronize with new technology while being resourceful, innovative and flexible.

Work Experience

Priyadarshini College of Engineering. *Nagpur, Maharastra*

Assistant Professor *May.2014 - Jun. 2018*

- Served the term of three years span as Assistant Professor Departmet of Electronics and Telecommunication and have taught the student's subject VLSI design,Digital Electronics,Analog Circuit Design and Digital Communication.I also played a major role as a part of core admission committee.

Krest Technologies *Pune, Maharashtra*

VLSI Trainee *Aug. 2014 - Jan. 2015*

- Worked as a trainee gaining the knowledge of backend designing in various CMOS technology in Cadence EDA and Tanner EDA.

Skills

Tools	Cadence (Virtuoso)EDA ,Tanner EDA, Autodesk Eagle, Altium Designer, Xilinx ISE
Front-end	Verilog, VHDL, TCL
Programming	Python, Basics of Embedded C, LaTeX
Software	Matlab, Pspice, Multisim
Digital marketing	SEO Analyst, Email marketing, Facebook ads
Website design	Wordpress

Projects

FOUR BIT MULTIPLIER AND 8 BIT ALU DESIGN USING BOOST LOGIC

Designed the Array multiplier, Baugh- Wooley multiplier and Wallace tree multiplier using adiabatic boost logic and compared to static CMOS Logic and design 8 bit ALU using boost logic. All simulations are done in Cadence Virtuoso using 45nm CMOS process Technology. The power consumption and the energy consumption found to be lesser than that of static CMOS logic and DPL logic.

VLSI DESIGN MULTIPLEXER USING REVERSIBLE LOGIC WITH 45NM

Design an ultra-area efficient multiplexer using reversible logic with 45nm technology with the help of reversible logic gates such as controlled not gate controlled controlled not gate, Feynman gate and Fredkin gate. Compare this multiplier with irreversible logic gate multiplier with different parameters such as power dissipation, time delay etc

BASIC CMOS CHOPPER AMPLIFIER

Designed CMOS chopper amplifier for very low frequency application. Chopping technique is an efficient approach to suppress the low frequency errors such as flicker noise or 1/f noise, drift and frequency offset of CMOS amplifier. This design and simulated at 180nm technology CMOS technology with 1.8v power supply

AUTOMATION IN SURVEILLANCE SYSTEM

Designed automation in surveillance system using AT89c51 microcontroller which sense number of people in class room and display to LCD and useful for commercial applications

Publications

- Vishal Shankarrao Muley, Anchu Tom and T Vigneswaran, "Design of Baugh Wooley and Wallace tree multiplier using two phase clocked adibatic static CMOS logic," IEEE Conference, 28-30 May 2015.
- Vishal Shankarrao Muley, Anchu Tom and T Vigneswaran,"DESIGN OF LOW POWER BARREL SHIFTER AND ROTATOR USING TWO PHASE CLOCKED ADIABATIC STATIC CMOS LOGIC",IJRET,Volume: 03 Issue: 09 | Sep-2014

Training and Workshops

ARAV system pvt ltd, Nagpur

Nagpur,Maharashtra

Trainee Engineer

Jun. 2019 - July 2019

- Worked as project trainee in ARAV System Pvt Ltd, and went through extensive training on LabVIEW programming language. Also learnt about LabVIEW interface with hardware controllers like myRIO , ELVIS, Arduino, ELVIS and other NI DAQmx devices.

Workshop

Nagpur,Maharashtra

Member

Jan. 2017

- Two week online ISTE STTP on CMOS, Mixed Signal and Radio frequency VLSI design by IIT Kharagpur at moodle centre Priyadarshini College Of Engineering, Nagpur.
- IEEE sponsored three day's workshop on "Arduino:Introduction and Hands on practice" held at Priyadarshini college of Engineering.
- One week ISTE STTP on Digital Signal Processing with applications using MATLAB and TMS 320 processor at Priyadarshini College Of Engineering, Nagpur.
- Organized and Delivered one day lecture on Introduction of Adibatic Logic design at Priyadarshini College of Engineering, Nagpur.

Accomplishment's

2008	**Topper of the batch during Diploma**, Shankarrao Dhawad Polytechnic College	*Nagpur*
2016	**Winner of Intercollegiate Carrom Championship**, Priyadarshini College of Engineering	*Nagpur*

Education

VIT University, Vellore

Vellore, Tamilnadu

Mtech in VLSI DESIGN

April. 2012 - Jun. 2014

- Accomplished the Masters Degree with 8.00 CGPA.

Shri Sant Gajanan Maharaj College of Engg, Shegaon

Shegaon, Maharashtra

Btech in Electronics and Telecommunication

Aug. 2008 - Jun. 2011

- Completed the Bachelor's Degree with 67.06 overall percentage.

Shankarrao Dhawad Polytechnic College,

Nagpur, Maharashtra

Engineering Diploma in Electronics and Telecommunication

July. 2005 - July. 2008

- Completed the Engineering Diploma with 77.76 (Honour) overall percentage.